shifting-clock). However, a more practical variation, shown in FIG. **14**, might be to incorporate both a counter and a shift register where the shift register would be used to enter an address onto the chip which could then be loaded into the counter. In this last variation of the serially loaded counter, the address would be retained within the counter so the many address lines are essentially reduced to four: one for the serial address input (S), one for clocking the shift register (K), one for clocking the counter (C), and one for loading the address into the counter from the shift register (L). One skilled in the art will quickly realize the circuitry needed to implement any of these variations. One well skilled in the art will recognize that a reduction to three lines can be achieved here resulting in a total of six connections to the chip (three plus power, ground, and data out).

Finally, a variation on the digital logic device comprising one or more DRS Arrays of which one or more may be removable which themselves comprise the above mentioned serially loaded counter logic. By limiting the manufacture of such devices to having output in analog format only, the risks to the makers of programming (e.g., music and video programs) will be reduced. With CD-ROM technology, the output from some CD-ROM readers is in a digital format. As a result, any copy made will be of the same quality as the original. This potentially results in significant lost revenue as the users of this technology could casually make copies for friends and relatives that cannot be distinguished from the originals (this was not the case with prior technologies such as cassette tapes and video tapes where each successive copy degraded somewhat). By limiting the manufacture of devices comprising DRS Arrays that are addressed via serially loaded counters to analog output only, the same degradation of copies will occur thereby reducing some of the risks to the makers of programming by causing the copies to be less desirable than the originals. While devices comprising DRS Arrays that are addressed via serially loaded counters could be limited to analog output only, they could still include means for reading DRS Arrays in other formats (i.e., DRS Arrays directly addressed via many address lines), however, devices comprising DRS Arrays that are directly addressed via many address lines and which give digital access to the information stored therein would not include means for reading DRS Arrays that are addressed via serially loaded counters.

It is believed that minor flaws in the semiconductor wafer will mostly impact the operation of the metal-on-silicon junction rectifiers when they are reverse biased by lowering the reverse breakdown voltage. Since the DRS Arrays are expected to be operated at low voltage levels, large reverse voltages are considered unlikely in normal operation. As a result, the impact of these minor flaws are not expected to impact the operation of the device and high device manufacturing yields are anticipated. However, the addressing transistors will likely be adversely affected by such flaws. There will likely be a trade-off between the increased cost of manufacture resulting from lowered device yields (as a result of the impact of semiconductor flaws on the increased complexity of the addressing circuit) and the savings on packaging (as a result of reducing the number of device leads).

The selection of a line by disabling all undesired lines could be utilized in many related electronic devices. The rectifiers at the storage locations could be fabricated as Light Emitting Diodes LED's) with such a rectifier present at every storage location. In this way, the device could be used as a display panel where a given display pixel could be turned on by selecting that bit location; the display panel would be scanned, selecting and illuminating bit locations in sequence while skipping bit locations that are to remain dark. Also, using a technique such as pulse width modulation, which is well known to one skilled in the art, one could even control the duration of a pulse of light emitted at any given pixel location and thereby control the perception of the intensity of the light emitted.

The high expected storage densities come from the symmetry the design—the Storage Bit Sensing Rectifiers, The Addressing Rectifiers, and the Storage Rectifiers are all constructed in the same way. The result of this is that they can all be made at the same time with the same semiconductor manufacturing steps. By using metal-on-silicon junction rectifiers, the primary components in the circuit are essentially constructed vertically on the semiconductor's surface instead of horizontally as might conventionally be done resulting in a very efficient use of the semiconductor "real estate". The scaling up of the device is expected to be easily accomplished. For example, on a one inch square chip, if the Anode Lines and the Cathode Lines are placed at roughly 0.45 micron center to center spacing, then a DRS Array that is roughly 65,536 by 65,536 Lines could be made. This is the equivalent of about 4,294,967,296 bits or about 536,870,912 bytes or about the capacity of a present day CD ROM. State of the art technology at the time of this writing is below 1 micron line widths. It is envisioned that the present invention could be used anywhere that one would use a CD-ROM drive or player or anywhere a large amount of information is needed.

The foregoing description of an example of the preferred embodiment of the invention and the variations thereon have been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

I claim:

**1**. A digital logic device comprising one or more electronic information storage means, and addressing means for accessing said storage means, wherein each said electronic information storage means comprises:

a plurality of generally parallel conductive means;

a second plurality of generally parallel conductive means that is generally perpendicular to and overlapping with the first said plurality of generally parallel conductive means;

a plurality of bits of potential information storage where a bit of said plurality of bits is present in the general vicinity of each point of intersection of each conductive means of the first said plurality of generally parallel conductive means with each conductive means of the second said plurality of generally parallel conductive means, and where the state of any said bit is determined by the presence or absence of a rectifying conductive means at each said general vicinity of said point of intersection;

means for selecting a conductive means of one plurality of generally parallel conductive means, and means for biasing the generally parallel conductive means of the other plurality of generally parallel conductive means such that each said rectifying conductive means present between a conductive means of said biased plurality of generally parallel conductive means to a conductive means of the other said plurality of generally parallel conductive means is potentially forward biased;

means for selecting a biased conductive means by electronically disabling conductive means within said biased plurality of generally parallel conductive means by shifting the voltage of those biased conductive means that are to be disabled; and

wherein said addressing means comprises:

means for controlling said means for electronically selecting conductive means of one said plurality of generally parallel conductive means and for electronically selecting conductive means of the other said plurality of generally parallel conductive means.

**2**. The digital logic device of claim **1**, wherein said means for selecting a conductive means of one plurality of generally parallel conductive means comprises:

means for biasing the generally parallel conductive means of the said one plurality of generally parallel conductive means such that each said rectifying conductive means present between a conductive means of said biased plurality of generally parallel conductive means and a conductive means of the other said plurality of generally parallel conductive means is potentially forward biased; and

means for selecting a biased conductive means by electronically disabling conductive means within said biased plurality of generally parallel conductive means by shifting the voltage of those biased conductive means that are to be disabled.

**3**. The digital logic device of claim **1**, further comprising means for detecting a conducted current through said rectifying conductive means if present at said point of intersection.

**4**. The digital logic device of claim **1**, wherein one of said plurality of generally parallel conductive means is a plurality of generally parallel doped regions within a semiconductor material.

**5**. The digital logic device of claim **4**, wherein the other of said plurality of generally parallel conductive means is a plurality of generally parallel metalized regions.

**6**. The digital logic device of claim **1**, wherein said addressing means comprises means to sequentially select addressed locations.

**7**. The digital logic device of claim **1**, wherein said addressing means comprises means to randomly select addressed locations.

**8**. The digital logic device of claim **1**, further comprising display means for displaying alphanumeric or graphic information to its user.

**9**. The digital logic device of claim **1**, further comprising input means to enable its user to alter its operation.

**10**. The digital logic device of claim **1**, wherein part or all of said one more electronic storage means are removable or replaceable.

**11**. The digital logic device of claim **1**, wherein output from the device is in a digital format.

**12**. The digital logic device of claim **1**, wherein output from the device is in an analog format.

**13**. The digital logic device of claim **1**, wherein output from the device is in either a digital format or an analog format

**14**. An electronic information storage device comprising:

a plurality of generally parallel conductive means;

a second plurality of generally parallel conductive means that is generally perpendicular to and overlapping with the first said plurality of generally parallel conductive means;

a plurality of bits of potential information storage where a bit of said plurality of bits is present in the general vicinity of each point of intersection of each conductive means of the first said plurality of generally parallel conductive means and each conductive means of the second said plurality of generally parallel conductive means, and where the state of any said bit is determined by the presence or absence of a rectifying conductive means at each said general vicinity of said point of intersection;

means for selecting a conductive means of one plurality of generally parallel conductive means, and means for biasing the generally parallel conductive means of the other plurality of generally parallel conductive means such that each said rectifying conductive means present between a conductive means of said biased plurality of generally parallel conductive means and a conductive means of the other said plurality of generally parallel conductive means is potentially forward biased; and

means for selecting a biased conductive means by electronically disabling conductive means within said biased plurality of generally parallel conductive means by shifting the voltage of those biased conductive means that are to be disabled.

**15**. The storage device of claim **14**, wherein said means for selecting a conductive means of one plurality of generally parallel conductive means comprises:

means for biasing the generally parallel conductive means of the said one plurality of generally parallel conductive means such that each said rectifying conductive means present between a conductive means of said biased plurality of generally parallel conductive means and a conductive means of the other said plurality of generally parallel conductive means is potentially forward biased; and

means for selecting a biased conductive means by electronically disabling conductive means within said biased plurality of generally parallel conductive means by shifting the voltage of those biased conductive means that are to be disabled.

**16**. The storage device of claim **14**, further comprising means for detecting a conducted current through said rectifying conductive means if present at said point of intersection.

**17**. The storage device of claim **14**, wherein one of said plurality of generally parallel conductive means is a plurality of generally parallel doped regions within a semiconductor material.

**18** The storage device of claim **17**, wherein said rectifying conductive means between said plurality of generally parallel doped regions and a plurality of generally parallel metalized regions is of the metal-on-semiconductor junction type.

**19**. The storage device of claim **17**, wherein said rectifying conductive means between said plurality of generally parallel doped regions and a plurality of generally parallel metalized regions is of the p-n junction type.

**20**. The storage device of claim **14**, wherein one of said plurality of generally parallel conductive means is a plurality of generally parallel metalized regions.

**21**. The storage device of claim **14**, wherein said rectifying conductive means is comprised by a transistor as the base-emitter junction.

**22**. The storage device of claim **14**, further comprising means for retaining the address of the information to be accessed.

**23**. The storage device of claim **22**, further comprising means for incrementing the retained address.

**24**. The storage device of claim **22**, further comprising means for setting the retained address.

25. An electronic information storage device comprising a plurality of storage means where each storage means comprises:

a plurality of generally parallel conductive means;

a second plurality of generally parallel conductive means that is generally perpendicular to and overlapping with the first said plurality of generally parallel conductive means;

a plurality of bits of potential information storage where a bit of said plurality of bits is present in the general vicinity of each point of intersection of each conductive means of the first said plurality of generally parallel conductive means and each conductive means of the second said plurality of generally parallel conductive means, and where the state of any said bit is determined by the presence or absence of a rectifying conductive means at each said general vicinity of said point of intersection;

means for selecting a conductive means of one plurality of generally parallel conductive means, and means for biasing the generally parallel conductive means of the other plurality of generally parallel conductive means such that each said rectifying conductive means present between a conductive means of said biased plurality of generally parallel conductive means and a conductive means of the other said plurality of generally parallel conductive means is potentially forward biased; and

means for selecting a biased conductive means by electronically disabling conductive means within said biased plurality of generally parallel conductive means by shifting the voltage of those biased conductive means that are to be disabled;

where at least one of said plurality of generally parallel conductive means is common to more than one said storage means.

26. The storage device of claim **25**, wherein said means for selecting a conductive means of one plurality of generally parallel conductive means comprises:

means for biasing the generally parallel conductive means of the said one plurality of generally parallel conductive means such that each said rectifying conductive means present between a conductive means of said biased plurality of generally parallel conductive means and a conductive means of the other said plurality of generally parallel conductive means is potentially forward biased; and

means for selecting a biased conductive means by electronically disabling conductive means within said biased plurality of generally parallel conductive means by shifting the voltage of those biased conductive means that are to be disabled.

27. A semiconductor information storage device comprising:

a plurality of generally parallel conductive means;

a second plurality of generally parallel conductive means that is generally perpendicular to and overlapping with the first said plurality of generally parallel conductive means where one of said two pluralities of generally parallel conductive means is generally a surface layer of the semiconductor; and

a plurality of bits of potential information storage where a bit of said plurality of bits is present in the general vicinity of each point of intersection of each conductive means of the first said plurality of generally parallel conductive means and each conductive means of the second said plurality of generally parallel conductive means, and where the state of any said bit is determined by the presence or absence of a rectifying conductive means at each said general vicinity of said point of intersection, and where any said presence or absence of a rectifying conductive means is determined by the leaving in place or the removal, respectively, of a portion of the surface layer conductive means

28. An electronic array of selectable points comprising:

a plurality of conductive means;

a second plurality of conductive means;

a plurality of selectable points where a point of said plurality of selectable points is present in the general vicinity of each point of intersection of each conductive means of the first said plurality of conductive means and each conductive means of the second said plurality of conductive means;

means for selecting a conductive means of one plurality of conductive means, and means for biasing the conductive means of the other plurality of conductive means such that each said selectable point present between a conductive means of said biased plurality of conductive means and a conductive means of the other said plurality of conductive means is potentially forward biased; and

means for selecting a biased conductive means by electronically disabling conductive means within said biased plurality of conductive means by shifting the voltage of those biased conductive means that are to be disabled.

29. The electronic array of selectable points of claim **28**, wherein said means for selecting a conductive means of one plurality of generally parallel conductive means comprises:

means for biasing the conductive means of the said one plurality of conductive means such that each said selectable point present between a conductive means of said biased plurality of conductive means and a conductive means of the other said plurality of conductive means is potentially forward biased; and

means for selecting a biased conductive means by electronically disabling conductive means within said biased plurality of conductive means by shifting the voltage of those biased conductive means that are to be disabled.

30. The electronic array of selectable points of claim **28**, wherein said each selectable point comprises a light emitting diode (LED) which will emit light when forward biased.

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